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(71) Applicant(s)

Simage Oy
(Incorporated in Finland)
Teknikantie 12, 02150 Espoo, Finland

(72) Inventor(s)

Stefan Jurthe
Marrku Tapio Eraluoto
Konstantinos Evangelos Spartiotis

(74) Agent and/or Address for Service

D Young & Co
21 New Fetter Lane, LONDON, EC4A 1DA,
United Kingdom

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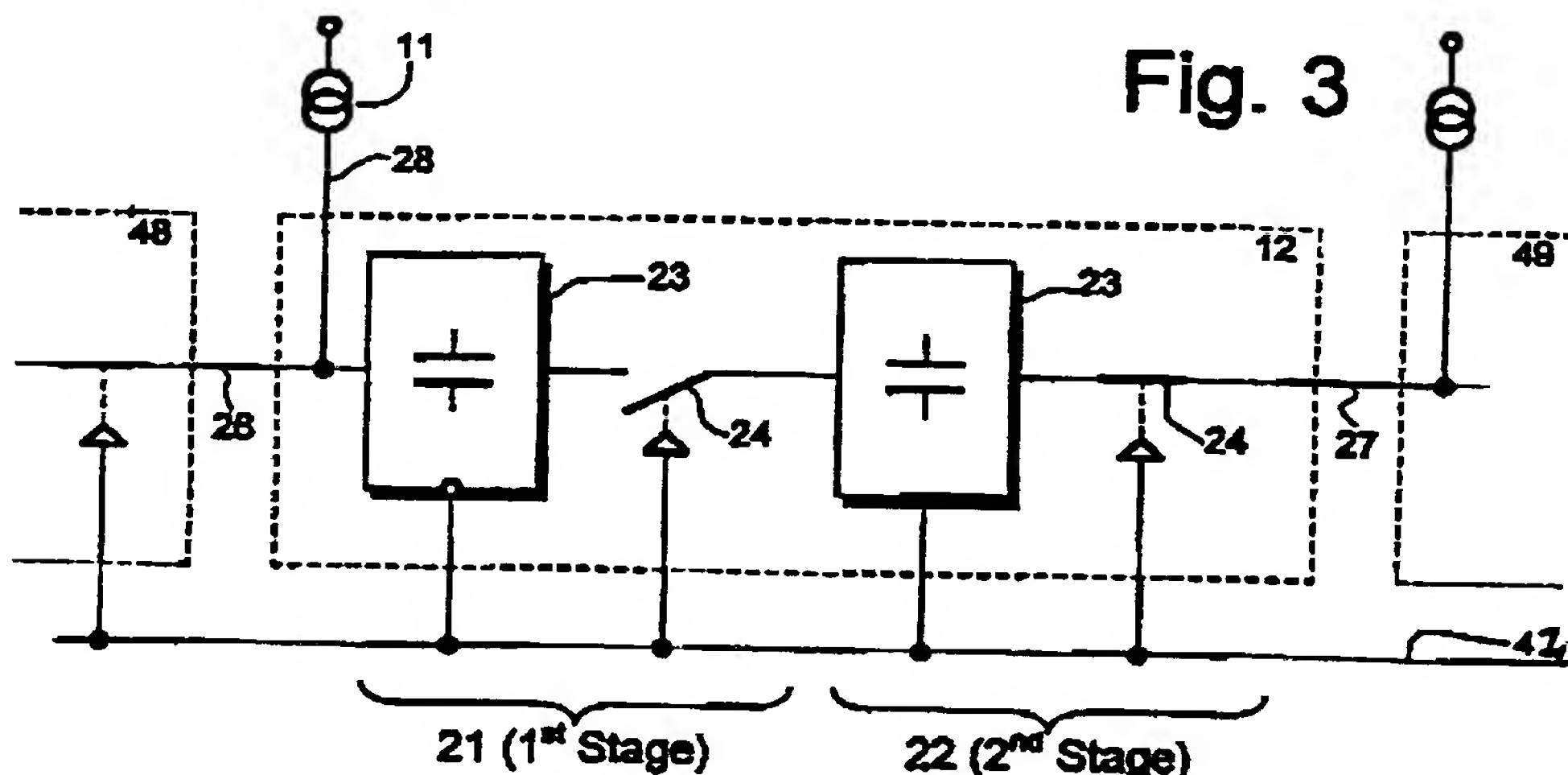
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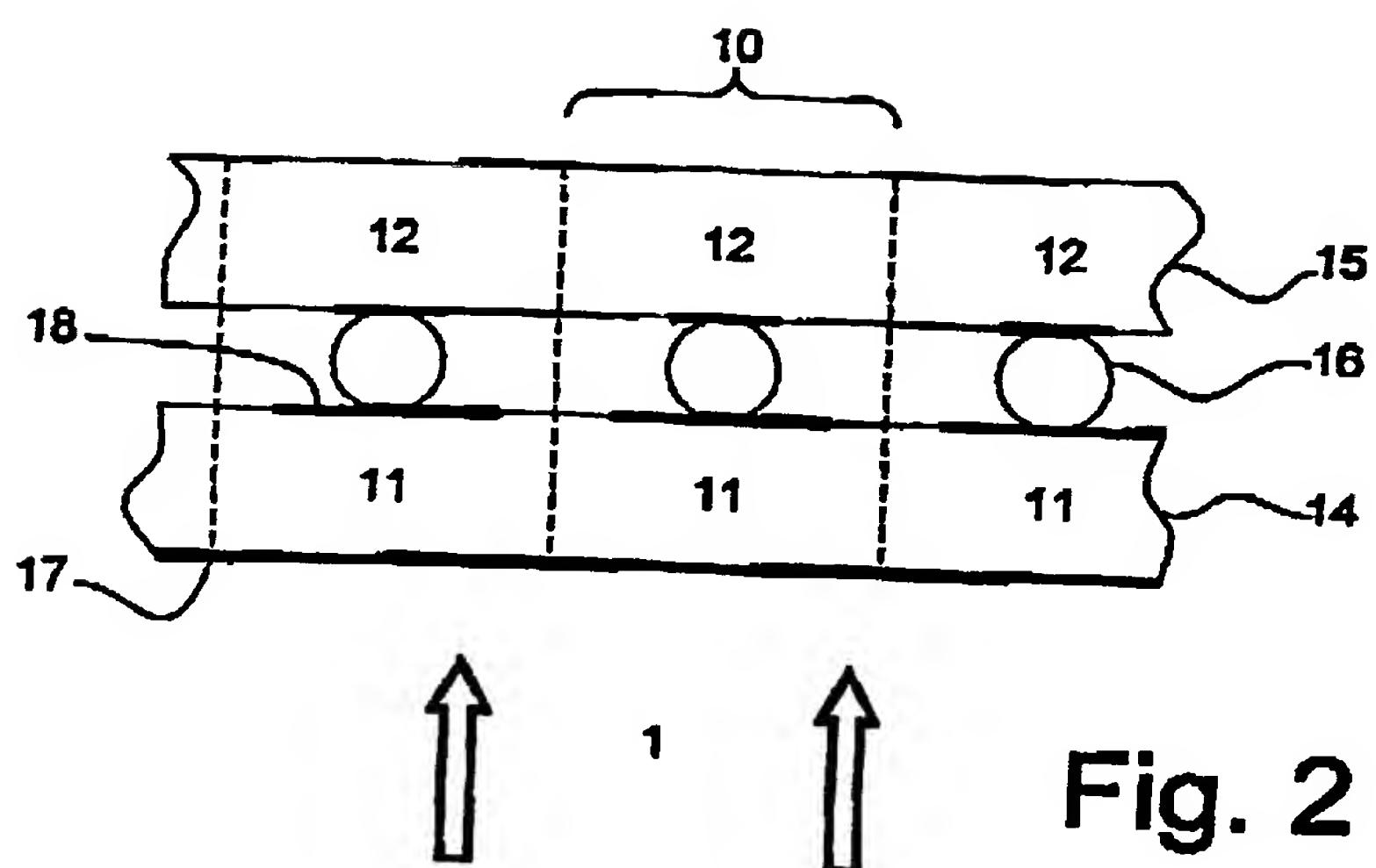
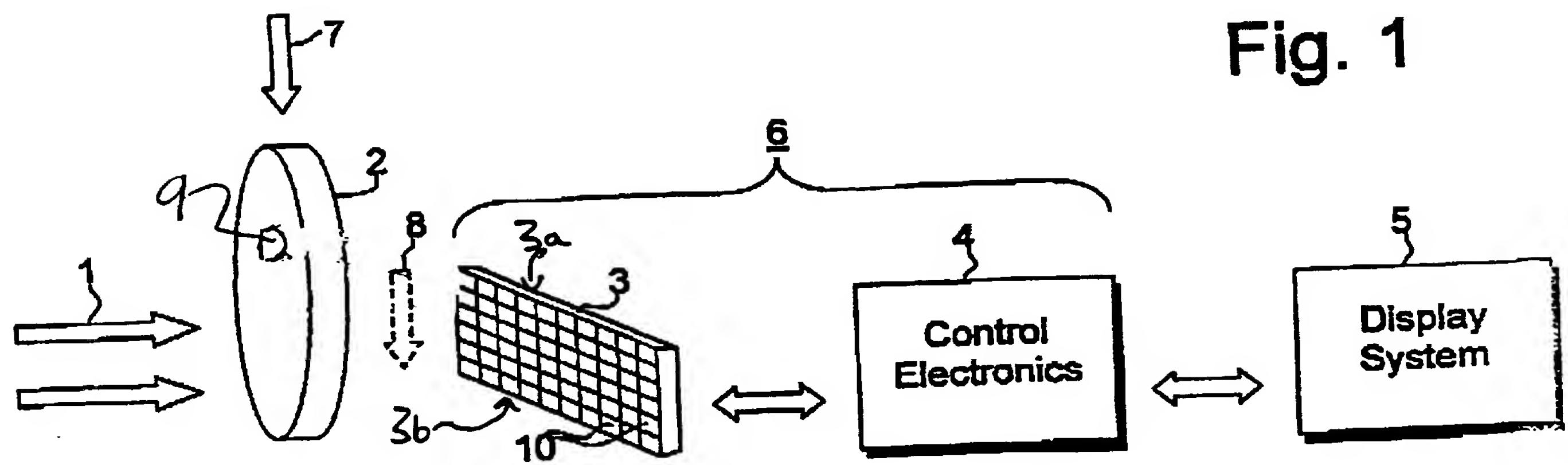
(54) Abstract Title

TDI scan Imager for direct-conversion radiation imaging

(57) An imaging device for scan-imaging radiation includes an array (3, fig.1) of detector cells 11 such as Active Pixel Imaging Device (ASID) cells or a Photon Counting Device (PCD) cells which generate charge in response to radiation incident directly upon them (e.g. X-, alpha-, beta- or gamma-rays). In an embodiment of the invention, charge is accumulated in a cell circuit, e.g. 12, associated with each individual detector cell 11. The cell circuits, 12 etc, are controlled so as to allow the accumulated charge from any one cell, e.g. 48 or 12, to be transferred to an adjacent cell, e.g. 12 or 49. By separating the accumulation and the transfer of charge into a first and a second stage, 21 and 22 respectively, each cell circuit is able to continue receiving charge from its associated detector cell 11 while transferring a previously accumulated charge packet and receiving another. Any charge accumulated during that stage is added to the charge received from the adjacent pixel circuit. Thus the device is permitted to continue receiving radiation generated charge from the cells 11 while performing time-delay and integration (TDI) of the accumulated charge. An image of an object (2) is reconstructed in a control electronics unit (4) and displayed on display a screen (5). In another embodiment using PCD methods, photon counts are accumulated in TDI mode rather than charge.



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Fig. 1**Fig. 2**

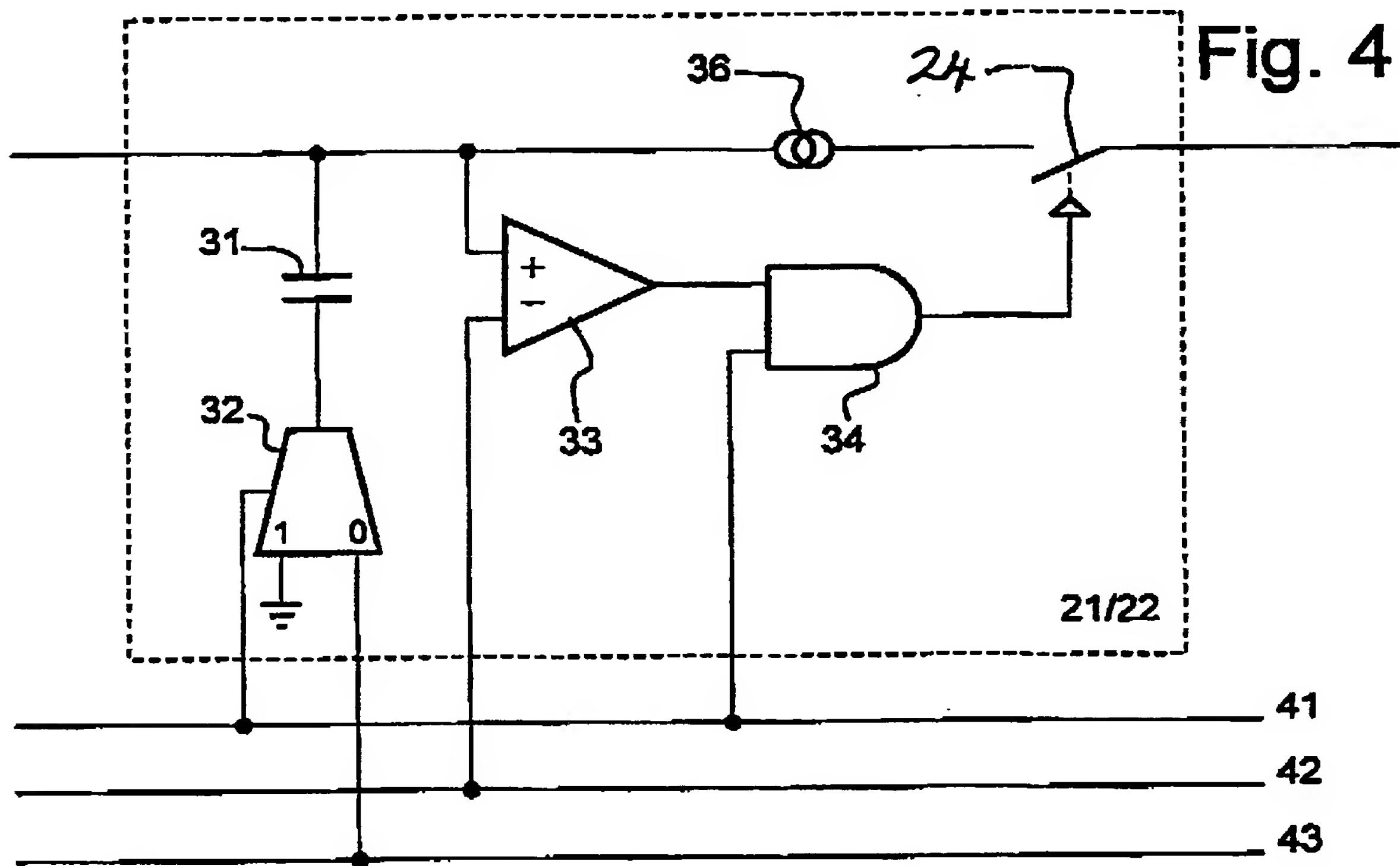
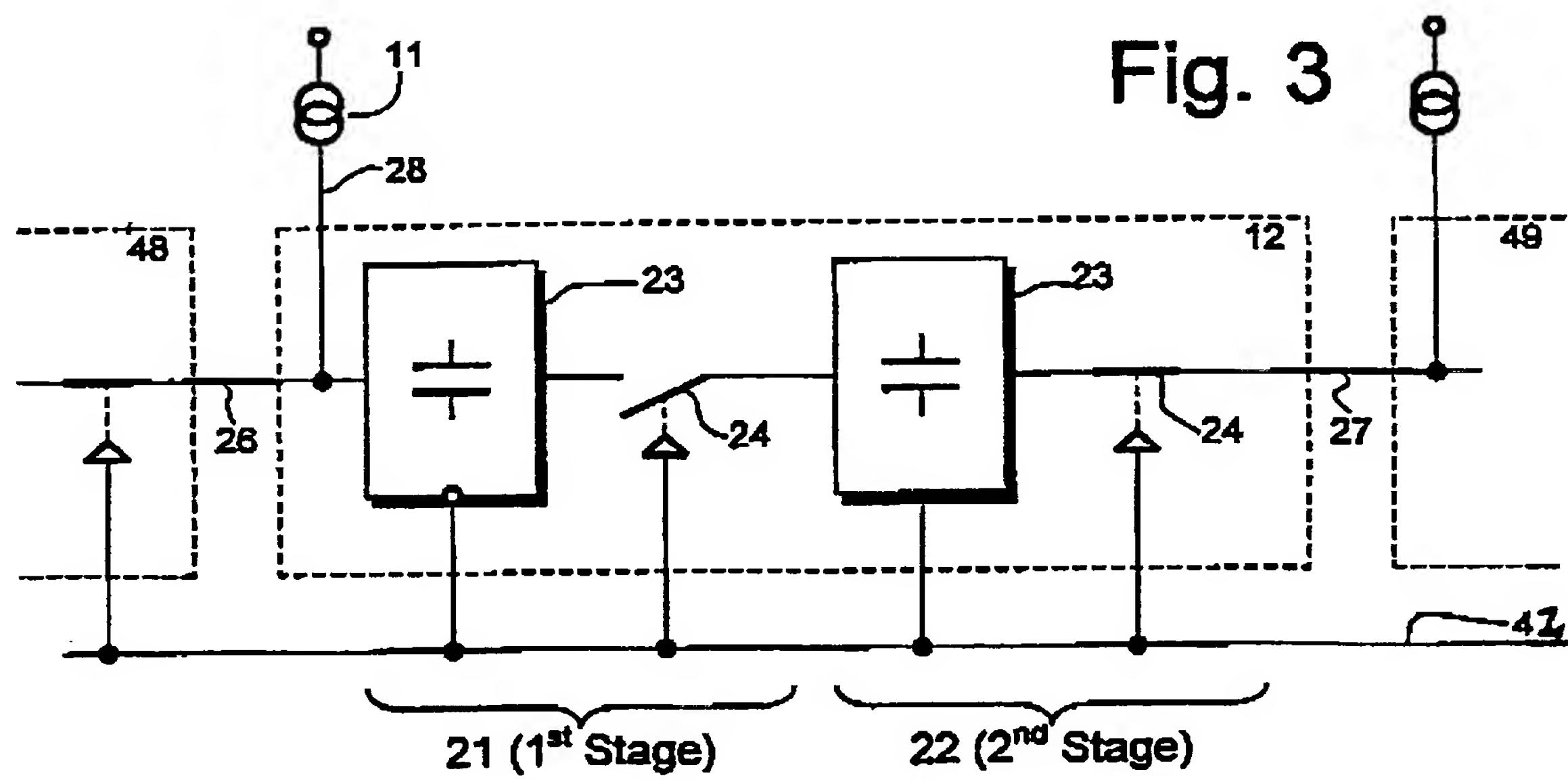


Fig. 5

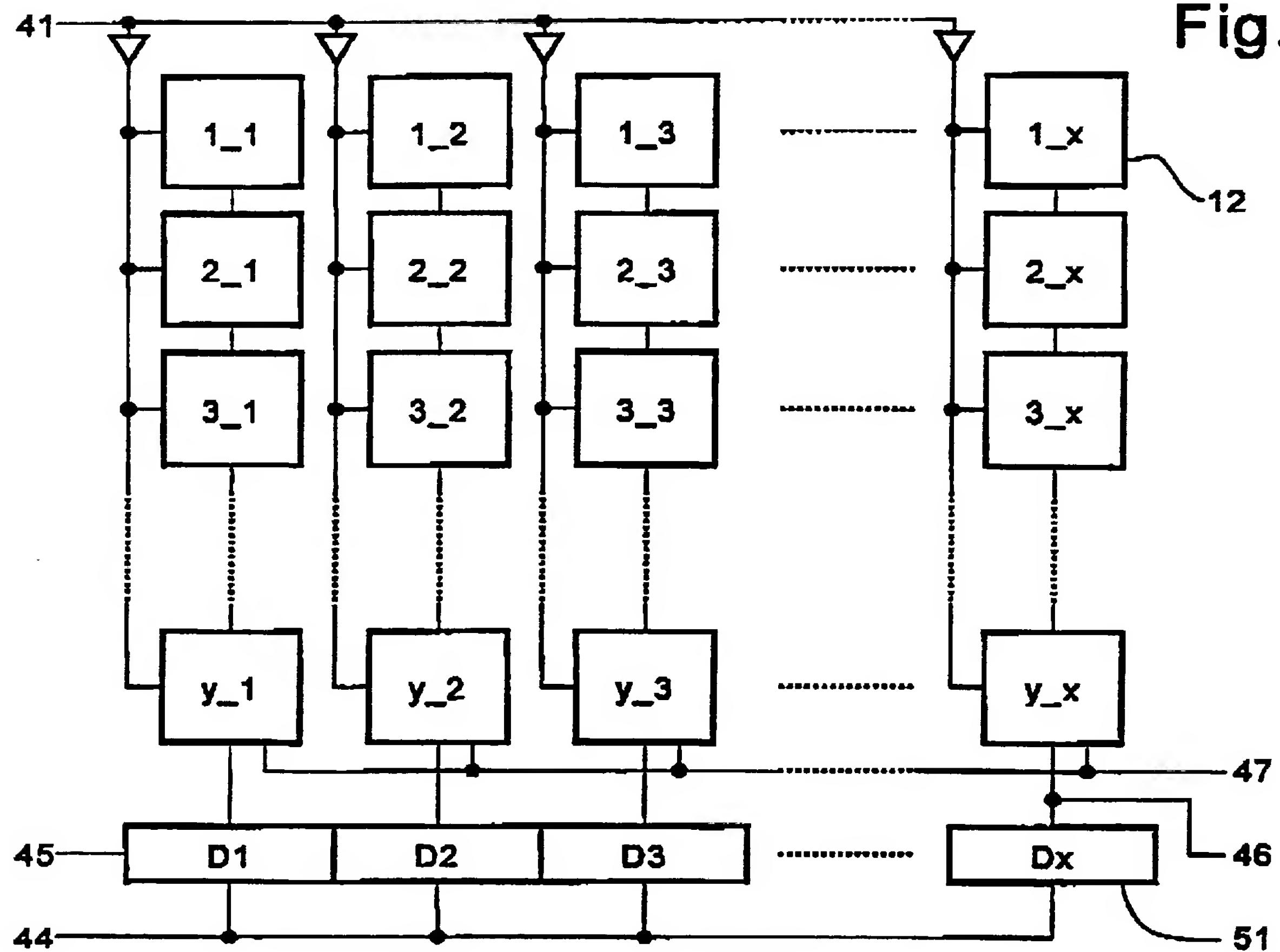


Fig. 6

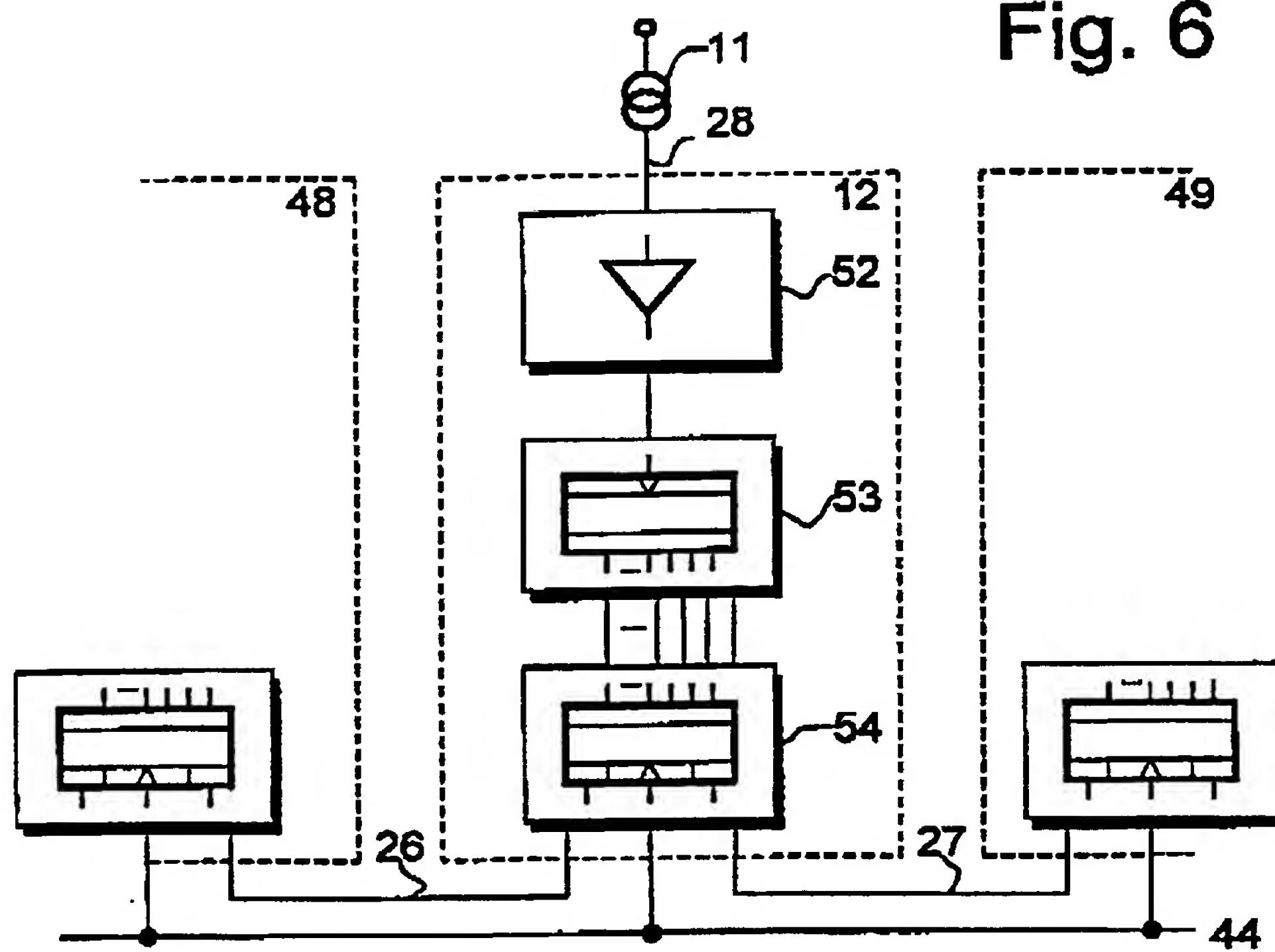


Fig. 7

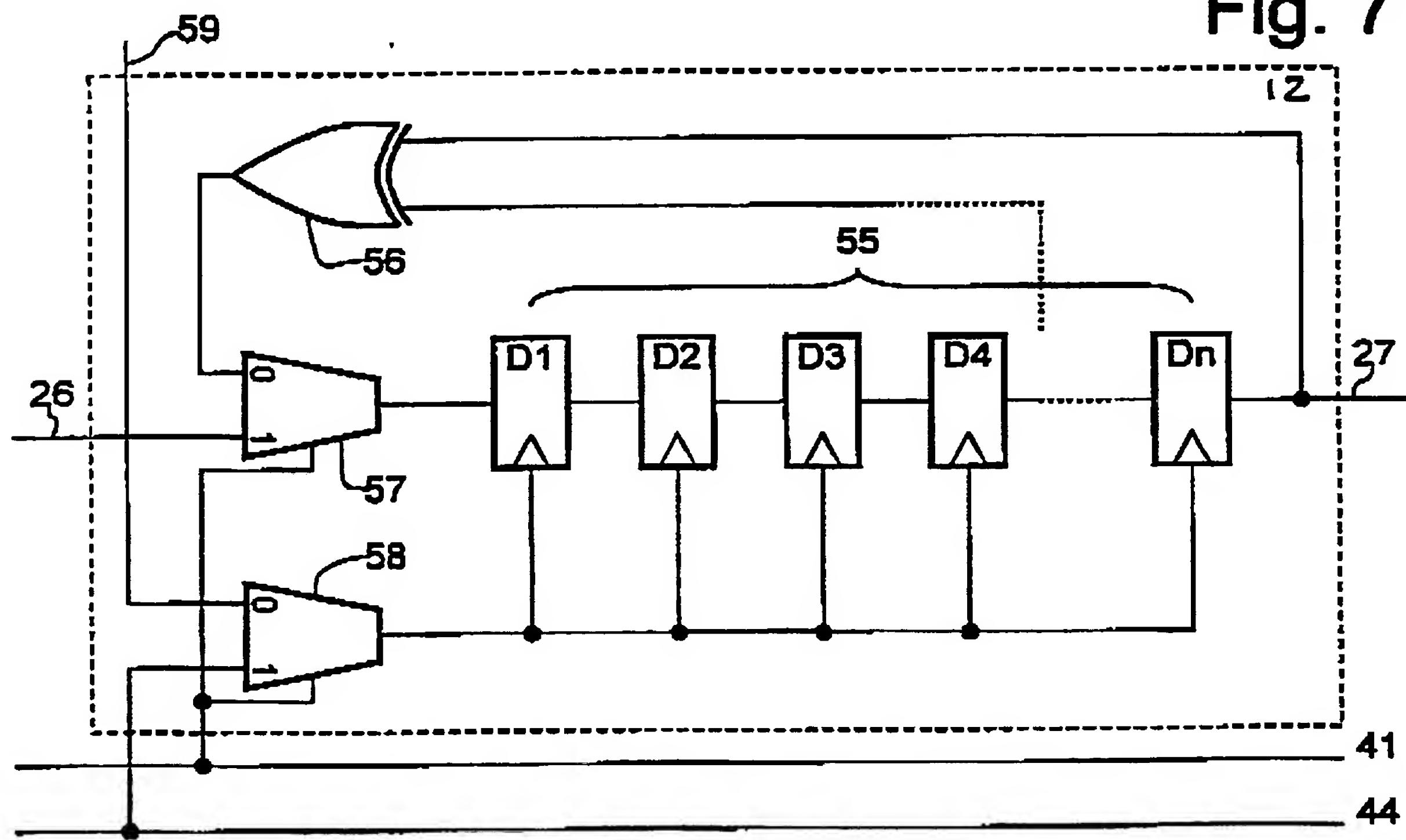
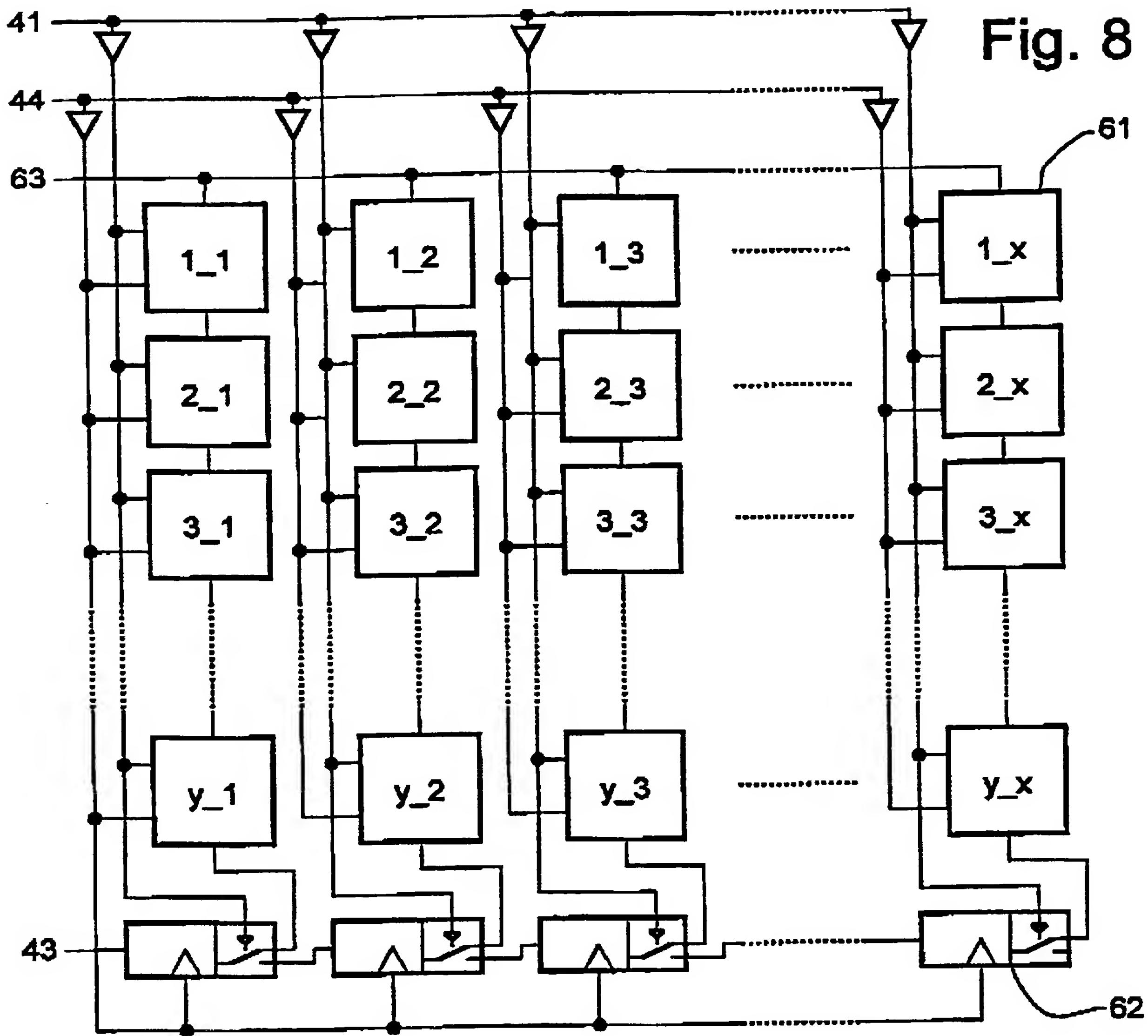


Fig. 8



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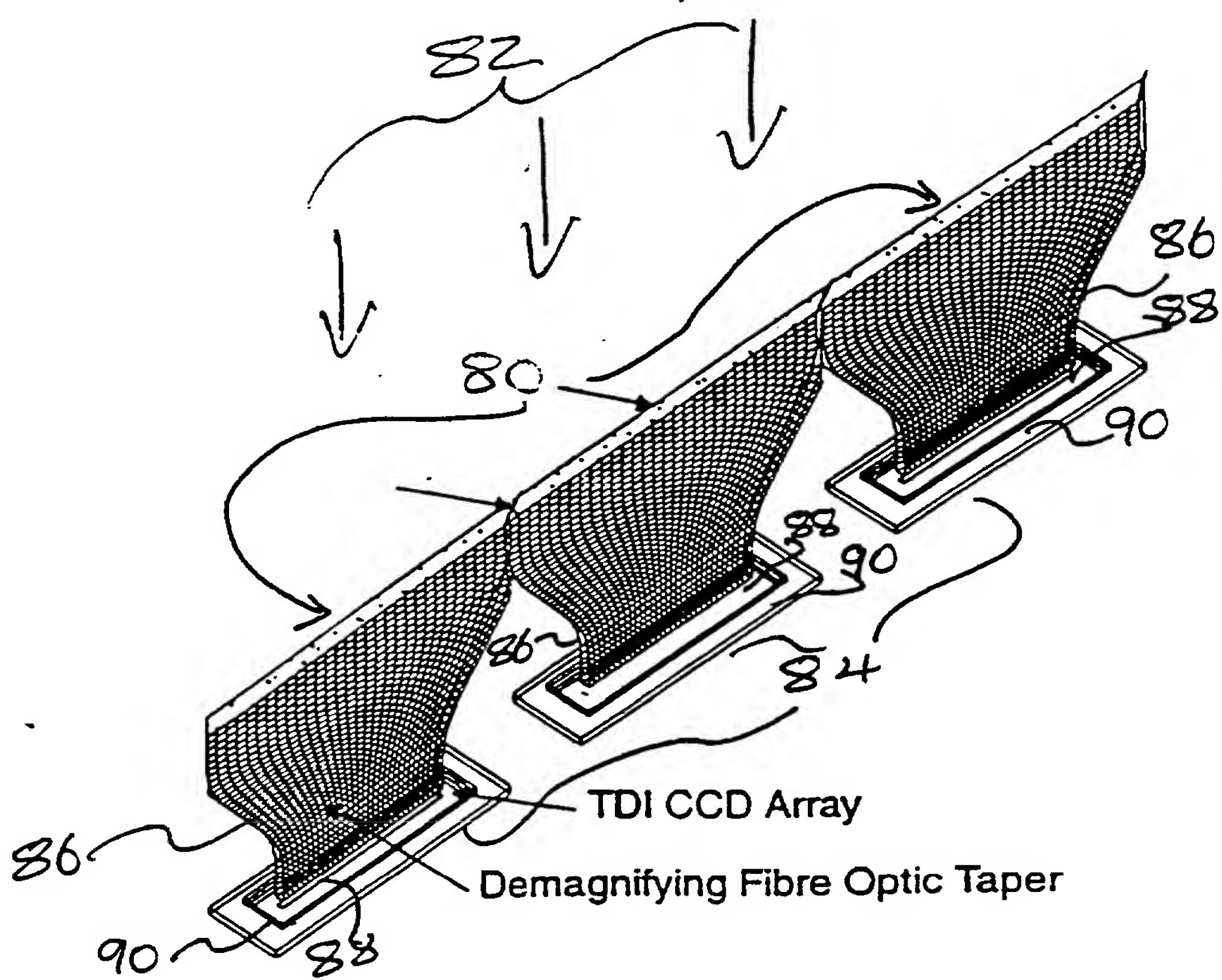


Fig. 9.

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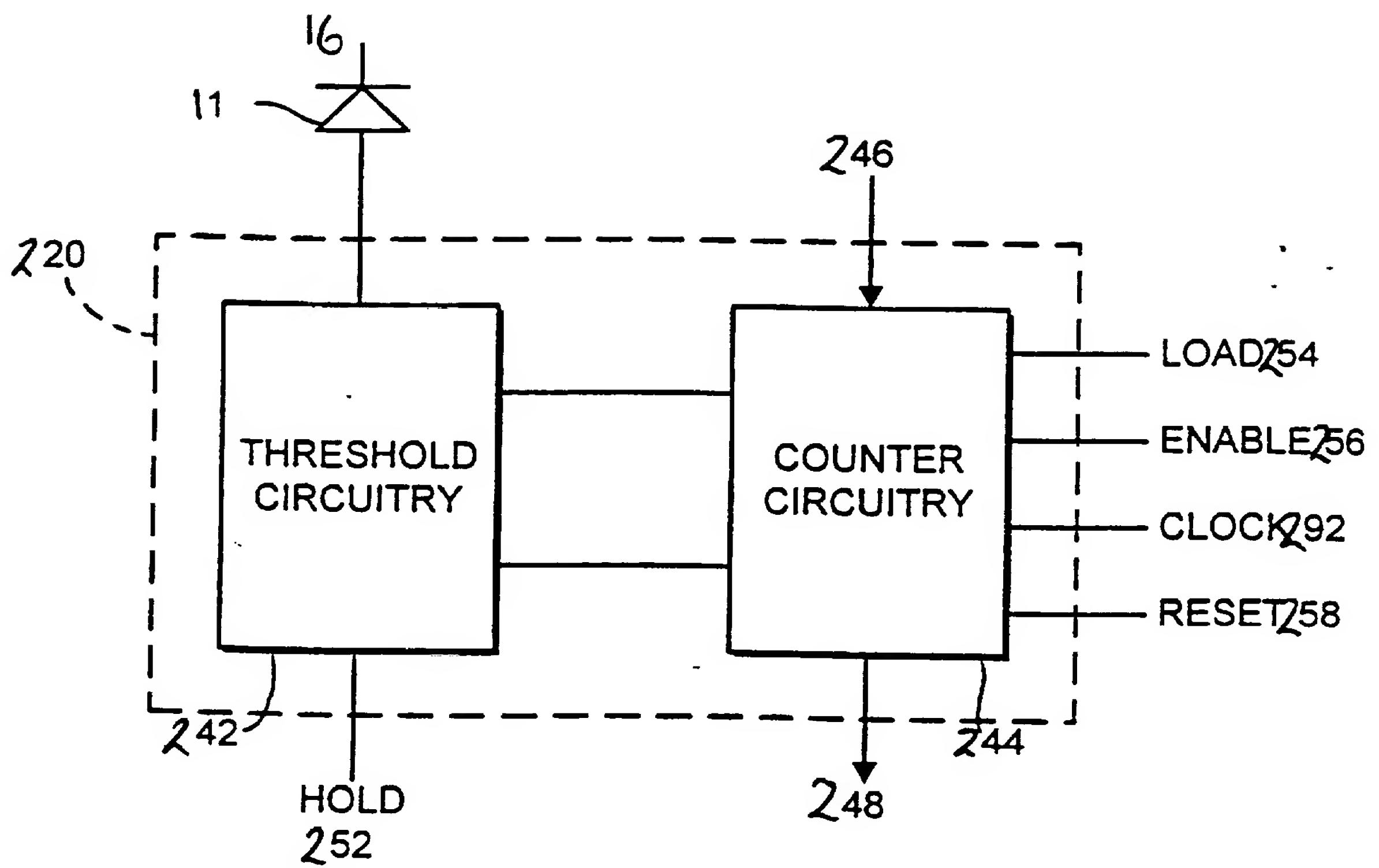


FIG. 10

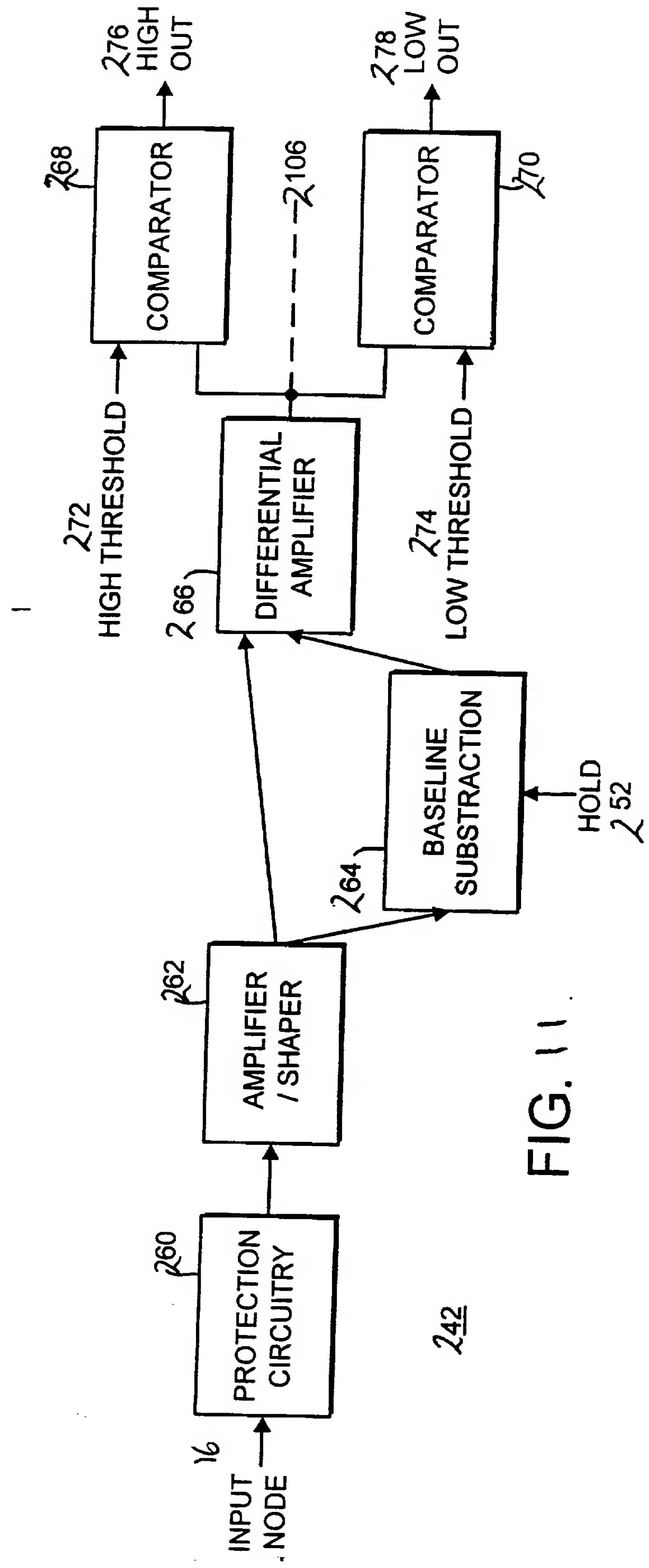


FIG. 11

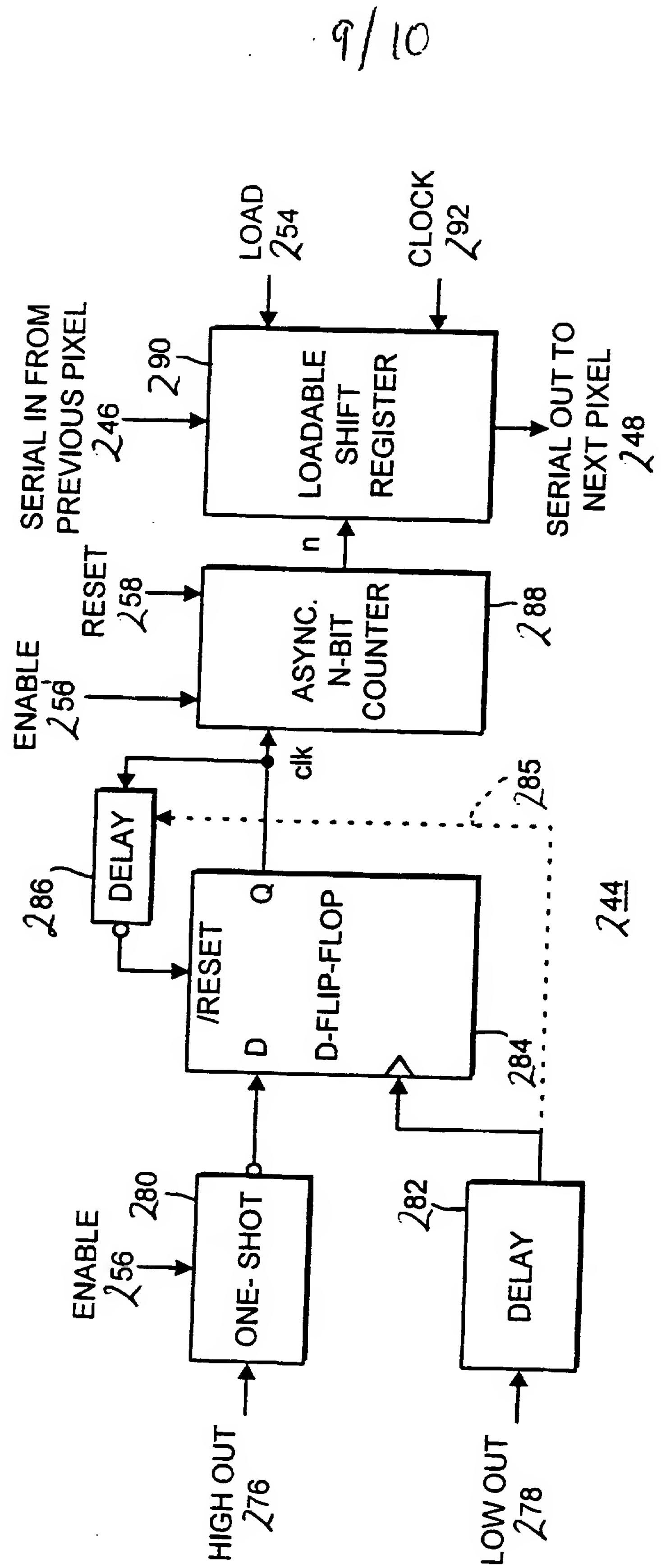


FIG. 12

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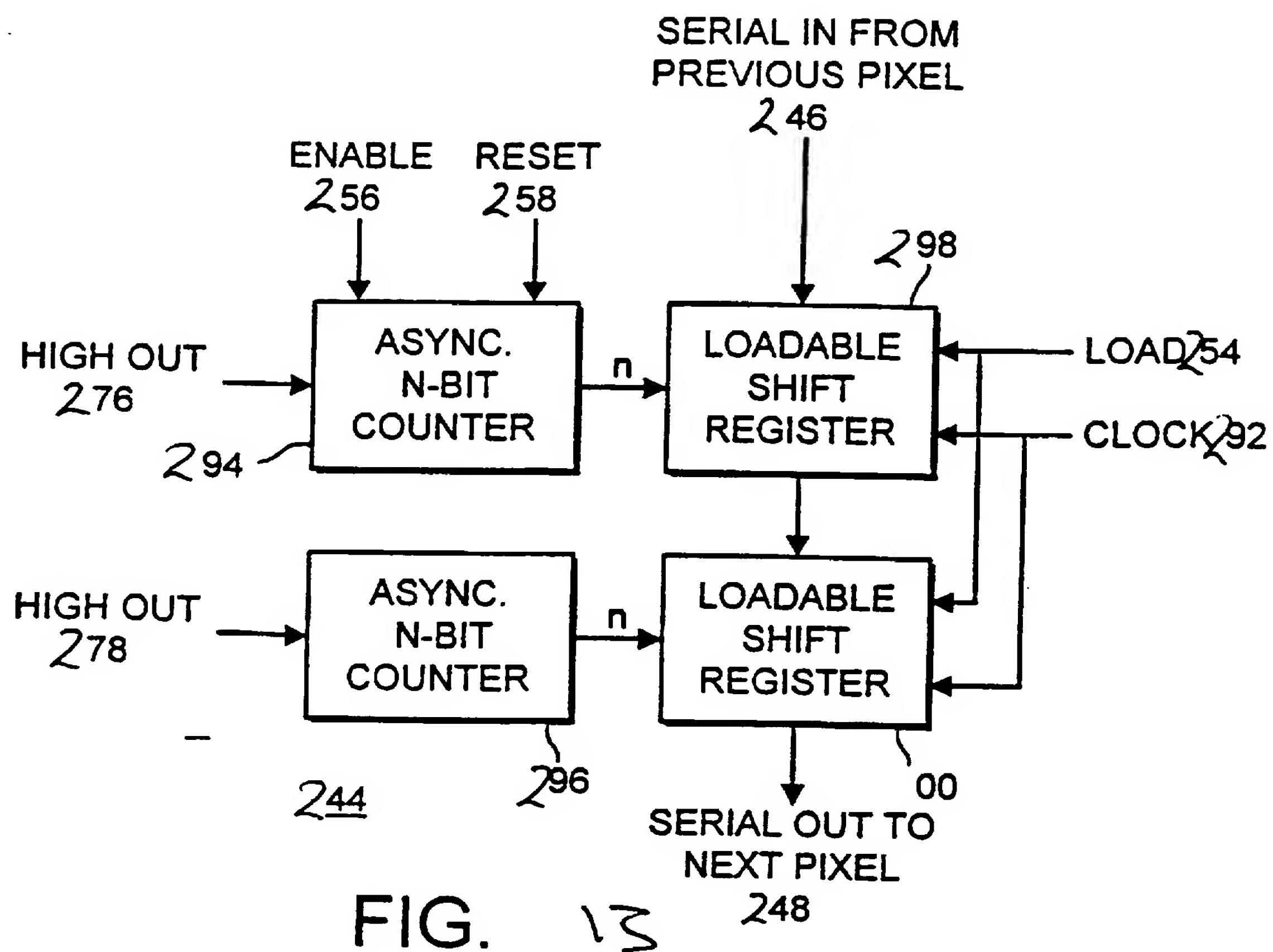


FIG. 13

Imaging Device

This invention relates to an imaging device for scan-imaging radiation, and in particular, but not exclusively, to an imaging technique known as Time Delay Integration (TDI).

5 Imaging devices comprising an array of pixels of various types are known and may or may not directly allow TDI mode of operation.

Charge coupled image sensors (also known as charge coupled devices (CCDs)) form one type of known imaging device. A CCD device operates in the following way.

10 1. Charge is accumulated in a depletion region created by an applied voltage. For each pixel the depletion has a potential well shape and constrains electrons under one electrode gate to remain within the semiconductor substrate.

15 2. Voltage is applied as pulse to the electrode gate of the CCD device to clock each charge to an adjacent cell. The charge remains inside the semiconductor substrate and is clocked through, pixel by pixel, to a common output. During this process no additional charge can be accumulated.

Another type of imaging device is the Active-pixel Semiconductor Imaging Device (ASID) described in International application publication number WO95/33332 and incorporated herein by reference. The ASID comprises an array 20 of pixels including a semiconductor substrate having an array of detector cells and a further array of pixel circuits. The detector cells generate charge in response to incident radiation. Each pixel circuit associated with a respective detector cell accumulates charge resulting from plural radiation hits of the associated detector cell. At determined times the charge from the pixel circuits can be read out and 25 used to generate an image based on the analogue charge values stored in each pixel circuit.

A further type of imaging devices are photon counting devices (PCD) described in International application publication number WO98/16853 and incorporated herein by reference. The PCD comprises an array of pixels including a 30 semiconductor substrate having an array of detector cells and a further array of pixel

circuits. The detector cells generate charge in response to incident radiation. Each pixel circuit comprises a discriminator registering radiation hits of a preferred energy range for a respective detector cell, and an n-bit digital counter and an n-bit loadable shift-register.

5 The PCD works in the following way.

1. The number of registered radiation hits in the associated detector cell is counted into the n-bit digital counter.

2. In response to an external request the value of the counter is loaded into the n-bit shift-register and the value of the counter is cleared.

10 3. All shift-registers of the entire sensor are chained and the information is clocked out in a serial fashion. Steps 1 and 3 can be executed simultaneously.

Of the afore-mentioned imaging techniques only CCD devices have been used in a TDI mode of operation since charge-shifting is an inherent feature of CCD technology.

15 Referring to Figure 9, there will now be described a TDI CCD detector and the operation of such a detector.

Since CCDs are sensitive only to visible light, a scintillator 80, such as a phosphor, for converting high energy radiation, such as X-rays 82, into visible light must be placed in front of the CCD device 84. The scintillator 80 is generally composed of a strip of phosphor material, and is coupled to a fibre optic taper 86, which is bonded to the active region 88 of the CCD device 84. Three fibre optic tapers 86 respectively bonded to three CCD devices 84 are illustrated in Figure 9. The fibre optic tapers 86 de-magnify light collection to provide space at the taper outputs to accommodate the outer non-active regions of the CCD devices 84, yet still maintain an acceptable light collection efficiency.

25 In a TDI mode, image acquisition takes place by scanning a continuously active X-ray beam across an object, such as a breast for mammography applications, and correspondingly moving the detector across the object, typically at the same scanning speed as the X-ray beam. Charge collected in CCD pixels is shifted down 30 the columns of the CCD devices 84 at a rate equal to, but in an opposite direction to,

the scanning X-ray beam. The charge packets collected at the end of the CCD columns have effectively remained stationary with respect to a given path of X-rays through the object, and they comprise the integral of several charge packets in the CCD column. This is because the sensor remains active at all times and the total 5 pixel charge on the image comes from integrating charge from multiple pixel cells as the total charge is clocked along one column. The collected charge packets are read out and typically digitised for processing into suitable images.

TDI mode imaging advantageously provides good total energy levels of imaging radiation and correspondingly good stability, yet from relatively low overall 10 X-ray illumination. Thus, providing good imaging whilst reducing the inherent danger from high power X-ray illumination.

However, CCD imagers require indirect conversion of X-rays to light, and thus have limited absolute sensitivity and resolution. Direct radiation to electron converting substrates cannot be connected to a CCD because the small pixel charge 15 capacity of CCDs saturates at very low doses of radiation, and cannot cope with the large currents provided by direct conversion.

The present invention seeks to mitigate the problems described in the prior art and embodiments provide a TDI imaging device not using a CCD.

In accordance with a first aspect of the invention there is provided an 20 imaging device for scan-imaging in a Time Delay Integration (TDI) mode comprising an image cell array including an array of detector cells for generating charge in response to incident radiation and a corresponding array of pixel circuits comprising accumulation circuitry for accumulating pixel image values corresponding to incident radiation, each pixel circuit being associated with a 25 respective detector cell and controllable to transfer a pixel image value to an adjacent pixel circuit.

Preferred embodiments of the invention provide for TDI mode imaging using detectors other than CCD devices, thereby avoiding the inherent drawbacks of such devices.

The pixel circuit is typically operable to receive a pixel image value from an adjacent (preceding) pixel circuit, which is loaded into the accumulation circuitry. The accumulation circuitry modifies, typically increases, the loaded pixel image value in accordance with radiation incident on said detector.

5 In a preferred embodiment the pixel circuit comprises transfer circuitry responsive to a control signal to transfer a pixel image value to a succeeding pixel circuit and to load a pixel image value from a preceding pixel circuit. Thus pixel image values representing radiation incident from a corresponding pixel element of an illuminated object can be accumulated and transferred along the pixel cell array,
10 in order to track radiation originating from that pixel element.

Preferably, the signal is a charge packet and the accumulation circuitry comprises a charge collector such as a capacitor coupled to the detector. The capacitor may be a CMOS capacitor, for example associated with an FET. Such a configuration advantageously utilises the circuit technology and elements of the
15 pixel circuits, without requiring special components.

Preferably, the transfer circuitry includes a second charge collector which receives a charge packet from the first charge collector during transfer of charge to a succeeding pixel circuit. Charge transfer is typically accomplished in at least two steps using both charge collectors in each step. The level of charge transferred is
20 determined by a reference voltage below which the charge on the first or second charge collector cannot fall. The reference voltage is generally internally generated, and can be a gate threshold voltage for example.

Suitably, the transfer circuitry comprises first and second switch means, typically transistors such as FETs or the like, respectively associated with the first
25 and second charge collection means. The switch means are operated in anti-phase to transfer charge from first and second charge collection means, and to an adjacent pixel circuit in a sequence of steps.

Typically, the accumulation circuitry is coupleable to a second charge collection means of a preceding pixel circuit for receiving and accumulating charge

from said preceding pixel circuit, and the second charge collection means is coupleable to accumulation circuitry of a succeeding pixel circuit.

Optionally, in a preferred embodiment of the invention the accumulation circuitry comprises counting circuitry for counting plural radiation hits incident on
5 an associated detector cell, and the pixel image value comprises a count value. Such an embodiment provides for the use of photon counting devices in TDI mode imaging.

Preferably, the accumulation circuitry further comprises threshold circuitry coupled to receive signals generated in said associated detector cell and having
10 values dependent on instant radiation energy, said counting circuitry being coupled to said threshold circuitry for counting radiation hits within a predetermined energy range or ranges.

More preferably, the transfer circuitry comprises a loadable register coupled to said counting circuitry for receiving a count value therefrom, and further
15 coupleable to respective loadable registers associated with said succeeding and preceding pixel circuits for receiving and forwarding count values to and from said succeeding and preceding circuits respectively. Typically, the loadable register is a shift register.

Advantageously, the counting circuitry and loadable register comprise logic
20 circuitry configured as a unitary element operable as the counting circuitry and the loadable register, which takes up less area on the pixel circuit substrate.

In a second aspect of the invention a preferred embodiment comprises a scanning imaging system comprising an imaging device as described above, control electronics for reading image information from said imaging device and processing
25 said imaging information for display, and display means for displaying said processed information. Suitably, the system comprises support means for said imaging device and said high energy radiation source and adapted to move said imaging device and high energy radiation source relative to an object disposed between said imaging device and high energy radiation source. Optionally, the
30 object may move relative to the radiation source and imaging device.

In a third aspect of the invention there is provided a method for operating an image cell array including an array of detector cells for generating charge in response to incident radiation and a corresponding array of pixel circuits comprising accumulation circuitry for accumulating pixel image values corresponding to incident radiation, each pixel circuit being associated with a respective detector cell and controllable to transfer a pixel image value to an adjacent pixel circuit, the method comprising receiving and transforming pixel image values from and to adjacent pixel circuits.

Suitably, the pixel image value is a charge packet.

In a preferred embodiment the method comprises electrically isolating a first charge collection means from a second charge collection means whilst receiving charge from a preceding pixel circuit and transferring accumulated charge to a succeeding pixel circuit, and subsequently electrically isolating the first and second charge collections means from the preceding and succeeding pixel circuits respectively and electrically coupling the first and second charge collection means for transferring accumulated charge therebetween.

Optionally, the method is for operating an imaging device wherein the accumulation circuitry comprises counting circuitry for counting plural radiation hits incident on the associated detector cell and the pixel image value comprises a count value, the method further comprising determining the charge from the detector fulfilling a predetermined criterion and correspondingly triggering the counting circuitry, for counting radiation hits within a predetermined energy range or ranges.

Exemplary embodiments of the invention will be described hereinafter, by way of example only, with reference to the accompanying drawings in which like elements have like numbers and in which:

Figure 1 is a schematic block diagram of an overall scan-imaging system configuration;

Figure 2 is a cross section of one example of a pixel array;

Figure 3 is a schematic block diagram of an analogue implementation of a pixel circuit of the imaging device in Figure 2;

- Figure 4 is an example circuit of one stage of the pixel circuit of Figure 3;
- Figure 5 is a readout configuration of an array of analogue pixel circuits;
- Figure 6 is a schematic block diagram of a digital implementation of a pixel circuit of the imaging device in Figure 2;
- 5 Figure 7 is an alternative example of the counter/shift register circuitry of the pixel circuit of Figure 6;
- Figure 8 is a readout configuration of an array of digital pixel circuits;
- Figure 9 is a schematic illustration of a conventional TDI CCD detector.;
- Figure 10 is a schematic illustration of an implementation of circuitry for
10 counting plural radiation hits;
- Figure 11 is a more detailed schematic illustration of the counting circuitry shown in Figure 10;
- Figure 12 is a schematic illustration of circuitry for counting radiation hits within a predetermined energy range; and
- 15 Figure 13 is a schematic illustration of further circuitry for counting radiation hits within a predetermined energy range.

Embodiments of the invention may use analogue (charge) accumulation and transfer when implemented with ASID pixel circuits, and alternatively digital (photon count) accumulation and transfer when implemented with PCD pixel
20 circuits. Both types of pixel circuits can be integrated using a standard wafer process (e.g. CMOS, NMOS, BICMOS) as well as future wafer processes.

In an analogue implementation, the pixel circuit comprises two capacitors, the first capacitor being connected to a respective detector cell. The pixel charge transfer employs additional circuitry whereby charge from the preceding pixel circuit
25 enters into the first capacitor and leaves the cell from the second capacitor as part of an accumulated charge packet.

The charge transfer is controlled by a single clock signal. Both capacitors with respective control circuitry form two similar stages controlled by complementary clock signals making one active and one inactive. Together with the

preceding and succeeding cell circuits a chain of active and inactive stages is formed e.g. along one column.

Charge transfer is realised by creating a voltage difference between two stages allowing current to flow from an active to an inactive stage and by precisely 5 switching off the current flow as a reference voltage on the capacitor of the inactive stage is reached.

From special cells at the end of the chains (e.g. columns) the charge can be read out and used to reconstruct an image based on the charge values accumulated.

In an alternative digital implementation the pixel cell circuit comprises a 10 discriminator responding with a pulse to a radiation hit of a desired energy threshold or range in the respective detector cell, an n-bit counter and an n-bit shift register. The inputs and outputs of the shift register are connected to the preceding and succeeding pixel circuit respectively forming a chain e.g. along one column. The counter and shift register can load in parallel from each other upon controls signals.

15 The TDI mode of operation in an array consisting of such cells can work in the following way:

1. Count values corresponding to radiation hits of the desired energy incident on the associated detector cell get added to the content of the counter.
2. The shift register loads the value from the counter and serial shifts it into 20 the register of the succeeding cell circuit.
3. The counter is loaded with a value from a preceding cell circuit from the shift register.

During Step 2 and 3 no radiation hits can be registered, thus, the pixel is inactive but the ration of inactive to active time may be better than 1 to 100.

25 From the last pixel circuit in a column the value can be read out and used to generate an image based on counted photons.

A more detailed description of embodiments of the invention will now be described.

Figure 1 is a schematic block diagram of one example of a scan-imaging 30 system using an imaging device 6 in accordance with an embodiment of the present

invention. This particular example is directed to the imaging of high energy radiation, e.g. X-ray radiation. However, it will be clear to persons of ordinary skill in the art that other radiation such as gamma radiation, alpha radiation or beta radiation for example may be used.

5 The imaging system of Figure 1 is shown to provide imaging of an object 2 moving at scanning speed V_{opt} 7 with respect to the pixel array 3 and subjected to radiation 1. The system of Figure 1 is shown with a moving object 2 in order to simplify and aid the clarity of the description of embodiments of the invention. Conventionally, the object, particularly, if it is part of the human body, is static and
10 the X-ray source and detector move relative to the object. Persons of ordinary skill in art will readily understand the principles described hereinafter and can adapt them for static objects. In this example the radiation 1 is X-ray radiation and the object 2 part of a human body. The pixel array 3 comprises a plurality of pixels 10 arranged in two dimensions. However, it will be appreciated that other embodiments may
15 have a different configuration (e.g. a strip arrangement).

Conceptually, a region of the object 2 may be considered to be a pixel element 9. Radiation impinging on pixel element 9 irradiates an area of pixel 3 corresponding to a pixel. As the object 2 moves relative to the pixel array 3 so the radiation corresponding to pixel element 9 impinges on succeeding pixels.

20 The imaging device directly detects incident X-ray radiation and accumulates at each pixel a pixel image value representing incident radiation from a corresponding pixel element 9 which moves from pixel to pixel cell 10, e.g. in a row by row fashion, with a speed V_{TDI} 8 which may be the same as V_{OPT} . The pixel image value starts with a value zero at the side 3a of the pixel array where the moving object 2 enters the field of view of the pixel array 3, and is read out after it reaches the opposing side 3b of the pixel array 3 where the object leaves the field of view. As a pixel image value moves through the pixel array 3 it accumulates a plurality a radiation hits corresponding to one point of interest on the moving object 2 rather than to one pixel on the pixel array.

Referring now to Figure 2, the pixel array 3 can be configured on a single semiconductor substrate (e.g. Silicon) with each pixel cell 10 comprising a detector cell 11 and a pixel circuit 12. Alternatively, the pixel array 3 can be configured on two substrates, one with an array of detector cells and one with an array of 5 corresponding pixel circuits, the substrates being mechanically and electrically connected by, for example, conventional bump-bonding technology or any other appropriate technology.

Figure 2 shows a schematic cross section of part of a pixel array 3. In this example, the pixel array 3 comprises a detector substrate 14 connected to a circuit substrate 15 by means of bump-bonds 16. A detector cell 11 of each pixel 10 is defined on the detector substrate 14 by a continuous electrode 17 which applies a biasing voltage and pixel location electrodes 18 to define a detection zone for the pixel 10. Corresponding pixel circuits 12 are electronically connected to the corresponding electrodes 18 by bump-bonds 16. In this manner, when charge is 15 generated in a detector cell 11 in response to incident radiation 1, the charge is passed via bump-bond 16 to the corresponding pixel circuit 12.

The actual size of the pixel cell will depend on the application for which the imaging device is intended, and will also depend on the integrated circuit technology available for constructing the pixel circuit 12 to be described later. With current 20 technology, it is not possible to obtain the smallest possible pixel cell sizes which would be required in some applications. Typically, the minimum pixel cell size is of the order 100 μ m square using current technology which is suitable for most diagnostic and dental imaging applications. However, with advances expected in circuit manufacturing technology it is expected that the minimum size can be 25 significantly reduced.

Accordingly, the present invention is not limited to any particular pixel cell size.

Any appropriate semiconductor material can be used for the substrates. For example, silicon may be used for the detector substrate and for the circuit substrate. 30 Other materials could be used, e.g the detector material could be selected from:

CdZnTe, CdTe, HgI₂, InSb, GaAs, Ge, TlBr, Si and PbI₂. The detector substrate need not be limited to direct conversion materials, but could comprise CMOS circuits, on a silicon substrate, and comprising photo-diodes for receiving light from a scintillator. Optionally, amorphous silicon can be used in conjunction with a scintillator screen and pixel circuitry including an active pixel circuit 120 as described hereinafter with reference to Figure 10.

Figure 3 is a schematic block diagram of an individual pixel circuit 12 in accordance with a first embodiment of the invention using analogue circuitry. The detector cell 11 is schematically represented by a radiation controlled current source in Figure 3. The input 28 to the pixel circuit 12 corresponds to the bump-bonding connection between the detector cell 11 and the pixel circuit 12. A further input 26 and an output 27 furnish connections to previous 48 and succeeding 49 adjacent pixel cell circuits. Charge can be exchanged between adjacent circuits in order to provide accumulated charge packet transfer from pixel cell to pixel cell.

When a photon is photo-absorbed in the detection zone of detector cell 11 creating electrical charge, or when a radiation particle ionises a detection zone of detector cell 11, an electric charge flows into the pixel circuit 12 through input 28. The detector charge is summed with any incoming charge from the preceding pixel circuit 48 entering through input 26. The combined charge can leave the cell through output 27 and enter the succeeding pixel circuit 49.

Each pixel circuit includes two similar series connected stages 21 and 22, comprising charge storing circuitry 23 and a switch 24 at the output of the stage, which although shown here separately can form a part of the charge storing circuitry 23. The switch is typically a semiconductor switch such as an FET for example. Charge passes through both stages under the control of a clock signal 41 which closes and opens the switches 24 of stages 21 and stage 22 mutually exclusively, or in anti-phases, and also activates and deactivates the stages respectively. Thus, a packet of charge is preceded and followed by a closed switch separating charge packages from each other.

The pixel circuit functions as follows.

1) In clock state 0 for clock signal 41 the switches 24 are in the states as shown, and charge from the preceding pixel circuit 48 together with charge from the detector cell 11 enters stage 21 where it is accumulated and summed. Charge on stage 22 belongs to the previous packet and is completely transferred to the 5 succeeding pixel circuit 49 over output line 27.

2) In clock state 1 for clock signal 41 all switches 24 are in the opposite state to that shown in Figure 3 and charge does not enter or leave pixel cell 12, instead all accumulated charge plus the charge still arriving from the detector cell 11 is transferred to stage 22.

10 Figure 4 shows a schematic circuit diagram for an implementation of stage 21 or 22 of Figure 3. The circuit comprises a capacitor 31 which is able to store the maximum expected pixel charge, and circuitry to manage the transfer of charge. One side of the capacitor 31 is connected to a clock controlled multiplexer 32 for switching between ground and a constant electrical potential 43 for transferring 15 charge between two capacitors in the form of an electrical current.

The switch 24 is also controlled by the AND-gate 34, as well as clock signal 41, which closes the switch 24 at clock state 1 of clock signal 41 only if the comparison of the capacitor voltage and the reference potential 42 shows that the capacitor voltage is greater than the reference potential. Thus, only exactly the 20 charge needed to reach reference potential on the capacitor is allowed to leave through the output.

As shown, the circuitry of Figure 4 operates as stage 21 shown in Figure 3. However, if the clock inputs of the AND-gate 34 and the multiplexer 32 are inverted, the circuitry shown in Figure 4 works as stage 22 shown in Figure 3. 25 Depending on the type of detector substrate and the required biasing voltage, the detector produces charge or discharge whereby the input polarity of the comparator 33 has to be as shown or inverted, respectively. Also, the constant potential 43 has to be smaller or greater than the reference 42, respectively.

The current source 36 is included in the schematic diagram shown in Figure 30 4 to limit the current which flows during the charge transfer and make it independent

from voltage drop and parasitic resistance. Therefore, the electrical potential on the capacitor 31 changes linearly improving the performance of the comparator 33. In practice, the current limitations can be provided by saturation of the switch 24.

Figure 5 is a schematic illustration of an x by y pixel array 3 consisting of 5 pixel circuits as described with reference to Figure 3, although not limited to such circuits. Cells of the yth and final row are different from the other cell circuits as that they have circuitry to read out the pixel value to a common output line 47 in response to a control signal which provided by a shift (address) register 51. The address register 51 is controlled by the readout clock 44 which has to be sufficiently 10 faster than the transfer clock 41 to shift pixel values of the yth row out before a next update of the yth row. That is to say, the readout clock must have a frequency at least 2y times great than the transfer clock 41. The readout cycle is started by an impulse of one readout clock cycle on input 45 and a similar impulse on the output 46 marks the end of the readout cycle.

15 Charge is accumulated and integrated at each pixel circuit location as the object 2 moves relative to the pixel array 3, and charge packets move down the array columns tracking their respective pixel element of the object 2. Eventually, the charge packets reach the yth row, where they are readout before the yth row is updated with the next accumulated charge packet.

20 Figure 6 is a schematic illustration of a block diagram for an alternative, digital, embodiment of a pixel circuit 12 of the imaging device in Figure 2. The pixel circuit 2 comprising a discriminator 52, an n-bit counter 53 and a n-bit shift register 54 providing a serial connection to a preceding 48 and succeeding 49 pixel circuit. The detector 11 is shown simplified as a radiation controlled current source.

25 When a photon is photo-absorbed in the detection zone of the detector cell 11 creating electrical charge, or when particle radiation ionises a detection zone of the detector cell 11, an electric charge flows into the pixel circuit through input 28. In response to a radiation hit of the desired energy range (e.g. excluding scattered radiation) the discriminator 52 produces a single pulse to be added to the value in the

counter 53. The counter value is representative of pixel luminance or radiation energy incident for that pixel.

Referring to Figure 6, under the control of control signals (not shown) the shift register 54 is loaded in parallel with the value from the counter 53. By 5 applying n clock cycles via the clock signal 44 the count value is serial shifted to the succeeding pixel circuit 49 over connection 27. A following control impulse loads a count value, shifted into register 54 from the preceding circuit 48, into the counter 53 and new radiation hits are accumulated and added to the value in the counter 53. For the time of the transfer cycle, i.e. transfer of count value from preceding and to 10 succeeding circuits, the detector is inactive. However, the active time may be more than 100 times greater than the transfer time and thus the inactive period does not significantly adversely affect the operation of the detector.

The implementation of the loadable counter 53 and the loadable shift register 54 in each pixel circuit requires a considerable amount of semiconductor area. 15 Therefore, a more efficient alternative is now described with reference to Figure 7.

Figure 7 shows a further embodiment implementing a counter and shift register with only an n-bit shift register 55 shown in Figure 7 comprising n D type flip-flops, two multiplexers and one XOR-gate with 2 or more inputs. The circuitry shown in Figure 7 functions as follows.

20 1) When the control signal 41 is at state 0 the input of the shift register 55 is an XOR combination of 2 or more flip-flop states (tabs of the shift register 55) and where the discriminator signal 59 output from discriminator 52 provides the clocking signal. In this configuration, the shift register 55 works as a pseudo-random number generator in which up to $2^n - 1$ different combinations (2^n for a 25 binary counter) of the register value are possible dependent on the position of the tabs.

2) When the control signal 41 is at state 1 the input of the shift register 55 of pixel circuit 12 is connected to the output 26 of the shift register of the preceding pixel circuit 48, and all registers are clocked by the clock signal 44. The 30 control signal 41 stays 1 for n clock periods of the clock signal 44 ensuring complete

transfer of the counter value to the next pixel circuit. Evidently, the shift register 55 cannot be updated by discriminator signal 59 during transfer of count values from and to respective preceding 48 and succeeding 49 pixel circuits.

- Figure 8 is a schematic illustration of an x by y array of digital pixel circuits.
- 5 If binary counters are used in the pixel circuits then the inputs of the first row of pixel circuits $1_1 \dots 1_n$ (signal 63) are connected to logical 0 to provide an initial counter value of 0. If the counter described with reference to circuit as Figure 7 is used, the input is a logical 1 giving an initial counter value of 111 ... 1 since a starting value of 0 would dead lock the pseudo random number generator used as a
- 10 counter in the circuitry illustrated in Figure 7.

The outputs of the pixel circuits $m_1 \dots m_n$ in the last row are of the array of Figure 8 are connected to an n-bit shift register 62 which that no transfer from the pixel cells between rows occur is connected in series over the entire row to serial shift out the all row values in the last through line 47 out of the pixel array, during

15 the time period.

Referring now to Figure 10 there is illustrated is a schematic diagram of an individual pixel circuit 220 suitable for implementing the counter 53 of Figure 6. The pixel detector 19 is represented by the diode 11 in Figure 6. The threshold circuitry 242 effectively filters input radiation intensity by comparing the input pulse

20 peak to one or more threshold values. The output of the threshold circuitry 242 is connected to counter circuitry 244 for counting pulses (radiation hits) within one or more predetermined ranges as defined by the threshold circuitry. The counter circuitry is connected to the shift register 54 and the shift registers of other adjacent pixel circuits for readout and count transfer purposes. Various inputs to the pixel

25 circuit 220 include hold 252, load 254, enable 256, reset 258 and clock 292 signal lines and voltage supply lines Vdd and Vss (not shown).

Figure 11 is a schematic block diagram of the threshold circuitry 242 represented in Figure 10. As shown in Figure 11, protection circuitry 260 is connected to the input node 16 (i.e the bump-bond connection 234 to the pixel detector 19). The protection circuitry is provided to prevent damage due to over-

under-voltage values and is typically provided by two diodes connected to the high and low supply line Vdd and Vss (not shown). The output of the protection circuitry 260 is connected to amplifier/shaper circuitry 262 which produces an analogue signal proportional to the charge injection of a delta peak. Preferably the amplifier shaper 5 262 is implemented by means of a charge sensitive amplifier followed by a shaper. The shaping time depends on the maximum signal rate on a pixel. Figure 11 illustrates optional baseline subtraction circuitry which is needed if the leakage current varies significantly within the selected shaping time. Optionally, one can select the time when the baseline is sampled. In this case, the baseline is sampled 10 outside normal measurement times.

A differential amplifier 266 subtracts the baseline so that comparators 268 and 270 see the true peak signal height. First and second comparators 268 and 270 have respective high and low threshold values 272 and 274 input thereto. The high and low threshold values can represent higher and lower limits of accepted signal 15 amplitudes. In this case any signal peaks below the low threshold and above the high threshold will be rejected by the counter circuitry 244. If the peak signal value exceeds the high threshold value 272, then the first comparator 268 outputs a logic 1, otherwise it outputs a logic 0.

Similarly, if the peak signal value exceeds the low threshold value 274, then 20 the second comparator 270 outputs a logic 1, otherwise it outputs a logic 0. It will be appreciated that the comparison output values of the present embodiment form one example only and in other embodiments of the invention other values could be output as a result of the comparisons.

Figure 12 is a schematic block diagram of a first example of counter circuitry 25 244. Depending on the shaping parameters and signal amplitudes, the high output signal 276 from the first comparator 268 always comes some time later than the low output 278 from the second comparator 270. In Figure 12, the high output 276 from the first comparator 268 is supplied to a one shot circuit 280 which is responsive to the enable signal 256. The low output 278 from the second comparator 270 is 30 supplied to a delay circuit 282. By applying a delay to the low output 278, the order

of the signals 276 and 278 can be reversed so that the signal received from the delay circuit 282 at the clock input C of a D-flip-flop 284 always comes later than the inverted output of the one-shot circuit 280 which is supplied to the D input of the flip-flop 284. If the high threshold 272 was not exceeded by the input signal,
5 the output Q of the flip-flop 284 will be set high. The output Q of the flip-flop 284 is connected via a delay 286 to a reset input RESET of the flip-flop 284 to cause the flip-flop to be reset after a delay D2 to ensure a minimum pulse length for the output "clk" signal from the Q output of the flip-flop 284. An alternative to feeding back the output Q to the delay 286 is represented by the dotted line 285 from the delay
10 circuit 282. Although a D-flip-flop 284 is shown in Figure 12, another type of flip-flop could be used.

The length of the single-triggered one-shot circuit 280 is adequate to coincide with the rising edge from the low output signal 278 from the second comparator 270 at all signals amplitudes.

15 The output "clk" from the output Q of the flip-flop 284 is provided as an input to an asynchronous n-bit counter 288. According to the type of counter used, counting can be disabled with an enable signal 256 before latching an n-bit output from the counter 288 to a loadable shift register 290. The counter 288 can then be reset and the counter 288 can be enabled to proceed with counting. Reading from
20 the pixel circuit can then be effected during the next counting period in response to the clock signal 292.

25 The overall operation of the triggered counter arrangements shown in Figure 12 is to cause a count to be accumulated in the counter 288 on each occasion that a signal is received in response to a radiation hit having an energy between the high and low threshold values 272 and 274.

An alternative arrangement for the counter circuitry is illustrated in Figure 13. In the alternative counter circuitry shown in Figure 13, both low and high output counts are directly obtained. This circuitry requires more circuit real estate and readout time than the circuitry of Figure 11, but it does allow a direct readout of
30 the number of counts between the thresholds by subtracting the low count from the

high count and also allows the output of the number of the counts higher than the high threshold by counting the high count only.

In Figure 13, therefore, an asynchronous n-bit counter 294 is connected directly to receive the high output of the first comparator 268. An asynchronous n-bit counter 296 is connected directly to receive the output 278 of the second comparator 270. In response to load signals 254, first and second loadable shift registers 298 and 200 can be loaded with the contents of the first and second asynchronous n-bit counters 294 and 296, respectively. As with the previous example, the contents of the loadable shift registers 298 and 200 can be transferred to a succeeding pixel circuit, and be loaded with the contents of a preceding pixel circuit shift register for initialising the counters.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention. For example, although specific embodiments of the invention have been described 15 with reference to Mammography, embodiments of the invention may also be used in chest x-ray radiography, Dental Panoramic Tomography and Non Destructive Testing and Evaluation, for example. Additionally, the object need not move, but the radiation source and detector can move. This is particularly important for scanning parts of the human body, and in tomography the linear speed of the 20 radiation source may not be matched by the linear TDI speed, i.e. speed of charge transfer, since it is the angular velocity of radiation source and the TDI speed which is to be kept constant. Although digital embodiments of the invention have been described with reference to serial coupled shift registers; it will be evident to a person of ordinary skill that the shift registers may be coupled in parallel.

25 The scope of the present disclosure includes any novel feature or combination of features disclosed therein either explicitly or implicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed by the present invention. The applicant hereby gives notice that new claims may be formulated to such features during the 30 prosecution of this application or of any such further application derived therefrom.

In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the claims.

CLAIMS

1. An imaging device for scan-imaging radiation in a Time Delay Integration (TDI) mode comprising an image cell array including an array of detector cells for generating charge in response to incident radiation and a corresponding array of pixel circuits comprising accumulation circuitry for accumulating pixel image values corresponding to incident radiation, each pixel circuit being associated with a respective detector cell and controllable to transfer a pixel image value to an adjacent pixel circuit.
10
2. An imaging device according to Claim 1, said pixel circuit operable to receive a pixel image value from an adjacent pixel circuit.
3. An imaging device according to Claim 2, said accumulation circuitry adapted to modify a received pixel image value in accordance with radiation incident on said associated detector cell.
15
4. An imaging device according to any one of Claims 1 to 3, said pixel circuit further comprising transfer circuitry responsive to a control signal to transfer a pixel image value from said pixel circuit to a succeeding pixel circuit and to load a pixel image value from a preceding pixel circuit to said pixel circuit.
20
5. An imaging device according to any one of Claims 1 to 4, wherein said pixel image value comprises a charge packet, and said accumulation circuitry comprises a first charge collection means coupleable to said detector for storing a charge packet corresponding to a pixel image value.
25
6. An imaging device according to Claim 5, wherein said transfer circuitry comprises a second charge collection means for receiving said charge packet from

said first charge collection means during charge transfer to a succeeding pixel circuit.

7. An imaging device according to Claim 6, wherein said accumulation circuitry
5 is coupleable to a second charge collection means of a preceding pixel circuit for receiving and accumulating charge from said preceding pixel circuit.
8. An imaging device according to Claim 6 or 7, wherein said second charge collection means is coupleable to accumulation circuitry of a succeeding pixel
10 circuit.
9. An imaging device according to any one of Claims 6 to 8, comprising first and second switch means respectively associated with said first and second charge collection means.
15
10. An imaging device according to Claim 9 operable to transfer said charge packet in first and second steps utilising said first and second charge collection means for each step.
- 20 11. An imaging device according to Claim 9 or 10, wherein said switch means are operable in anti-phase for transferring said charge packet between adjacent pixel circuits.
- 25 12. An imaging device according to any one of Claims 5 to 11, wherein said first and/or second charge collection means comprises a capacitor.
13. An imaging device according to Claim 12, wherein said first and/or second charge collection means comprises a CMOS capacitor.

14. An imaging device according to Claim 13, wherein said CMOS capacitor comprises a capacitance associated with an FET.
15. An imaging device according to any one of Claims 5 to 14, wherein an amount of charge transferred between pixel circuits is controllable by a voltage comparison with respect to a reference voltage.
16. An imaging device according to Claim 15, wherein said reference voltage is internally generated.
- 10
17. An imaging device according to Claim 15 or 16, wherein said reference voltage is a gate threshold voltage.
- 15
18. An imaging device according to any one of Claims 1 to 4, wherein said accumulation circuitry further comprises counting circuitry for counting plural radiation hits incident on said associated detector cell, and said pixel image value comprises a count value.
19. An imaging device according to Claim 18, wherein said accumulation circuitry further comprises threshold circuitry coupled to receive charge generated in said associated detector cell and having values dependent on incident radiation energy, said counting circuitry being coupled to said threshold circuitry for counting radiation hits within a predetermined energy range or ranges.
- 20
- 25
20. An imaging device according to Claim 18 or Claim 19, further comprising transfer circuitry comprising a loadable register coupleable to said counting circuitry for receiving a count value therefrom, and further coupleable to respective loadable registers associated with succeeding and preceding pixel circuits for receiving and forwarding count values from and to said succeeding and preceding circuits respectively.
- 30

21. An imaging device according to Claim 20, wherein said loadable register is coupleable to said counting circuitry for loading said counting circuitry with a count value from said preceding circuit
- 5 22. An imaging device according to Claim 20 or 21, wherein said loadable register is a shift register.
- 10 23. An imaging device according to any one of Claims 20 to 22, wherein said counting circuitry and loadable register comprise logic circuitry configured as a unitary element operable as said counting circuitry and said loadable register.
- 15 24. An imaging device according to any of Claims 2 to 23 controllable to transfer said pixel image value between pixel circuits of adjacent rows of said array of pixel circuits at a speed V_{TDI} = pixel row spacing multiplied by a transfer frequency.
- 20 25. An imaging device according to Claim 24, adapted to read said pixel image value from a last row of said array of pixel circuits at a frequency at least equal to said transfer frequency multiplied by the number of pixel circuits in said row.
- 25 26. An imaging device according to any preceding Claim, wherein said detector cells comprise a direct-conversion material for directly converting incident radiation into charge.
27. An imaging device according any preceding Claim, wherein said detector cells are sensitive to high energy radiation such as X-rays, and/or gamma rays, and/or alpha rays, and/or beta rays.
- 30 28. A scanning imaging system comprising an imaging device according to any preceding Claim, and further comprising control electronics for controlling said device and reading image information from said imaging device, a processor for

processing said image information for display, and display means for displaying said processed information.

29. A scanning imaging system according to Claim 28, further comprising a high
5 energy radiation source disposed confronting said imaging device.

30. A scanning imaging system according to Claim 29, further comprising support means for said imaging device and said high energy radiation source and adapted to move said imaging device and high energy radiation source relative to an
10 object disposed between said imaging device and high energy radiation source.

31. A method for operating an imaging device for scan-imaging in a Time Delay Integration (TDI) mode said imaging device comprising an image cell array including an array of detector cells for generating charge in response to incident radiation and a corresponding array of pixel circuits comprising accumulation circuitry for accumulating pixel image values corresponding to incident radiation, each pixel circuit being associated with a respective detector cell and controllable to transfer a pixel image value to an adjacent pixel circuit, said method comprising receiving a pixel image value from an adjacent pixel circuit.
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32. A method according to Claim 31, further comprising transferring a pixel image value from said pixel circuit to an adjacent pixel circuit.

33. A method according to Claim 31 or 32, further comprising modifying a
25 received pixel image value in accordance with radiation incident on said associated detector cell.

34. A method according to any one of Claims 31 to 33, wherein said pixel image value comprises a charge packet.

35. A method according to Claim 34, further comprising accumulating charge received from said associated detector cell and from a preceding adjacent pixel circuit in a first charge collection means.
- 5 36. A method according to Claim 35, further comprising transferring an accumulated charge from said first charge collection means to a second charge collection means.
- 10 37. A method according to Claim 36, further comprising transferring said accumulated charge from said second charge collection means to a first charge collection means of a succeeding adjacent pixel circuit.
- 15 38. A method according to Claim 37, comprising electrically isolating said first charge collection means from said second charge collection means whilst receiving charge from a preceding pixel circuit and transferring accumulated charge to a succeeding pixel circuit, and subsequently electrically isolating said first and second charge collections means from said preceding and succeeding pixel circuits respectively and electrically coupling said first and second charge collection means for transferring accumulated charge therebetween.
- 20 39. A method according to any one of Claims 31 to 33 for operating an imaging device wherein said accumulation circuitry comprises counting circuitry for counting plural radiation hits incident on said associated detector cell and said pixel image value comprises a count value, the method further comprising determining said charge fulfilling a predetermined criterion and correspondingly triggering said counting circuitry for counting radiation hits within a predetermined energy range or ranges.

40. A method according to Claim 39, further comprising transferring a count value to a succeeding pixel circuit and receiving a count value from a preceding pixel circuit.

5 41. A method according to Claim 40, further comprising initialising said count circuitry with said received count value, and increasing said count value in accordance with incident radiation.

10 42. A method according to any one of Claims 31 to 41, further comprising transferring said pixel image value between adjacent circuits at a speed V_{TDI} equal to 10 the pixel separation multiplied by a transfer frequency.

15 43. A method according to Claim 42, further comprising reading said pixel image value from a last row of said array of pixel circuits at a speed sufficient to complete said reading prior to a next update of pixel circuits of said last row.

44. An imaging device substantially as hereinbefore described with reference to respective embodiments and accompanying drawings.

20 45. An imaging system substantially as hereinbefore described, with reference to respective embodiments and accompanying drawings.

46. A method substantially as hereinbefore described, with reference to respective embodiments and accompanying drawings.



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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H4F (FCCF, FCCY, FHHC, FHHD, FHHX); H5R (RAL, RTD)

Int Cl (Ed.6): H04N (3/14, 3/15, 5/32, 5/335)

Other: Online databases: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2323736 A	(Northern Telecom) See whole document. NB page 8 & fig.5.	1-10, 12-16,26, 31-37.
X	US 5402168	(Thomson) See whole document. NB col.6 and fig.3.	1-10,12, 13,26,28, 31-37.
X	US 5315114	(Texas) See col.3 lines 9-42 and fig.1.	1-10,12, 31-38.
X	US 5113263	(Audaire) See line 50 of col.2 to line 49 of col.3 and fig.4.	1-10,12, 31-38.

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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